Design and Performance of Additively Manufactured In-Circuit Board Planar Capacitors

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***Abstract*— This article discusses the design and performance of planar capacitors built as pairs of conductive plates by additive manufacturing as part of an electronic circuit board. This article covers several geometries and layers of parallel plates that allow for different capacitance values, from a few picofarads (pF) to several nanofarads (nF). The dc, ac, and radio frequency (RF) characterization demonstrated superior performance compared to off-the-shelve surface mount device (SMD) capacitors up to 20 GHz. The additively manufactured capacitors exhibit breakdown voltages in excess of 1 kV and subpicoampere leakage currents, while the change in RF impedance changes, as a function of frequency, is a factor of 3× smaller than SMD capacitors.**

***Index Terms*— Additively manufactured electronic (AME) devices, capacitors, capacitors ac and radio frequency (RF) performance, printed capacitors, *Q*-factor.**

I. Introduction

ADDITIVELY manufactured electronic (AME) devices are becoming attractive for the capability to integrate and embed components within the electronic circuit without the need to solder mount such components. Furthermore, AME enables embedding of integrated circuits (ICs), passive, and active components within a single package/board, as indicated in the 2019 Heterogeneous Integration Roadmap (HIR) [1]. Currently, high-frequency capacitors are individually packaged, soldered chip capacitors, with the exception of semiconductor ICs. However, for the semiconductor IC, the maximum capacitance values are very small due to sizes of the die, which prevents the ability to control electromagnetic compatibility (EMC) performance for radio frequency (RF) circuits. In RF printed circuit boards (PCBs) or other packaged structures, one of the most challenging areas is how to improve the EMC performance, especially in small circuit boards. For PCBs, EMC performance is managed by adding RF signal adsorbent elements, which adds complexity to the fabrication process. While additive manufacturing or 3-D printing has been previously used for fabrication of parallel-plate capacitors [2]–[4], the techniques used limit the size and flexibility to monolithically integrate these capacitors in an electronic circuit or the solutions have not been suitable for commercial manufacturing. Recent work on AME bandpass filter uses capacitors fabricated with the same technology as the capacitors presented in this article [5].

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This article describes the design and performance of planar capacitors fabricated with multimaterial and multilayered additive manufacturing technology, enabling capacitors with different areas and different layer counts resulting in capacitance values from a few picofarads (pF) to several nanofarads (nF). Furthermore, this article overviews AME capacitors in terms of standard capacitors, from dc to RF, allowing designers to utilize those capacitors in different electronic circuits application that could benefit from these capacitors and eliminate the need to mount them as part of the component assembly process in commercial circuit boards. The results show a consistent relationship between theoretical and experimental capacitance values. Since the capacitors are an internal part of the circuit, parasitic capacitances, resistance, and induction from soldering are eliminated, thus minimizing the equivalent series resistance (ESR) and equivalent series inductance (ESL) values, especially for RF applications. This demonstrates that AME capacitors behave close to an ideal capacitor, which is a superior performance when compared to surface mount technology (SMT) capacitors, which reduces and could eliminate the need for added EMC absorbent materials.

II. Design and Tests

A. Design of Multilayer Additively Manufactured Planar Capacitors

Planar capacitors are made from parallel conductive layers in the XY plane with dielectric layers between them in the Z-axis, as shown in Fig. 1. The theoretical capacity of n dielectric layers connected in parallel is given by

$$C = \epsilon_0 \times \epsilon_r \times \frac{A}{d} \times (n-1) \quad (1)$$

where A is the area of each electrode plane, d is the dielectric thickness between two electrode plates, γ_0 is the dielectric

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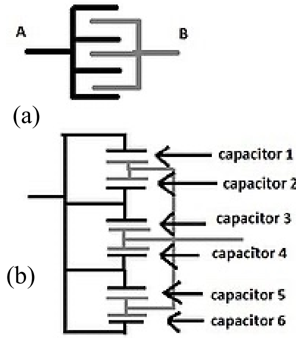


Fig. 1. (a) Capacitor plates pairs as parallel capacitor. (b) Parallel capacitor circuit as implemented in this study.

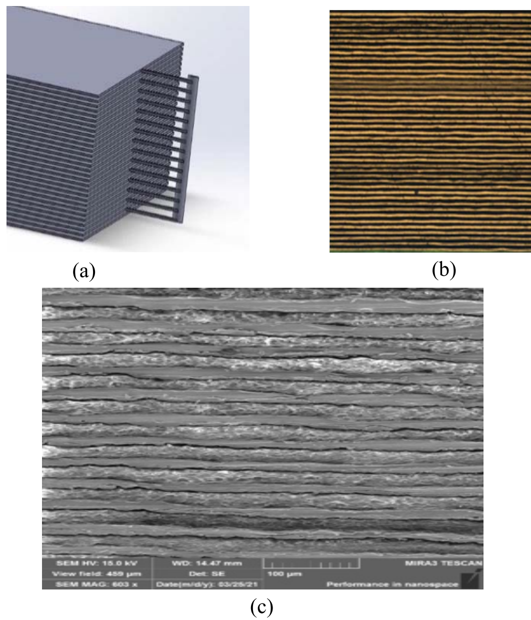


Fig. 2. (a) Computer-aided design view of a multilayer capacitor showing the dielectric, conductive layers, and one of the vias that connect the corresponding layers. (b) Cross-sectional view of an actual 55 layers capacitor structure, dark layers are the dielectric. (c) SEM close-up view of a section of the capacitor of (b).

permittivity, γ_r is the dielectric constant, and n is the layer count.

For this study, all metal layers in a capacitor have the same area. The conductive layers are alternately connected to a corresponding via on the side of the capacitor for connection to the circuit [Fig. 2(a)]. The connection to the circuit can be made on any layer of the AME device as needed by the designer. Due to the 3-D nature of these capacitors, a mechanical 3-D CAD software was used to create the print file. In the future, such capability should be available in electronic CAD design software to facilitate the use by commercial circuit designers.

The capacitor structure in Fig. 2(b) was fabricated in a Nano Dimension's DragonFly lights-out digital manufacturing (LDM) system. This system uses inkjet for simultaneous deposition of two types of materials, conductive ink (CI) based on silver nanoparticles and dielectric ink (DI) based on photopolymers. The system simultaneously builds multilayer 3-D designed circuit devices and boards for electronic applications

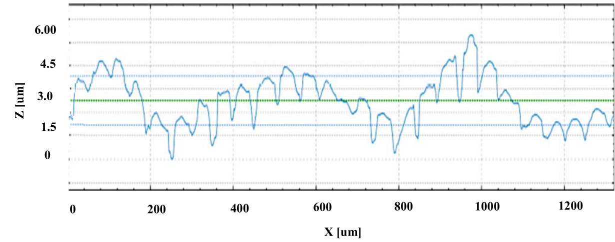


Fig. 3. Profilometer top surface roughness.

from the bottom-up. The simplicity of changing the structure of each printed layer allows for the creation of difficult or impossible to fabricate structures using standard manufacturing of PCBs. In addition, the capacitors are integrated into the device/board, eliminating the need to mount them as part of the component assembly.

The current fabrication capability of the DragonFly LDM provides for the following minimum capacitor design parameters.

1) Minimum conductive layer thickness: 17 μm.
2) Minimum dielectric layer thickness: 35 μm.
3) Number of dielectric layers: 1–55.

The materials used for this work are proprietary inks developed and optimized by Nano Dimension for use in conjunction with their AME fabrication system, where both inks operate at a viscosity between 10 and 15 cps [6]. The process conditions for the fabrication are summarized as follows.

1) Chuck temperature: 140 °C.
2) UV for polymerizing the DIs.
3) IR at 0.85 kW over 10-mm linewidth for drying and sintering the silver nanoparticle CI.
4) Stage speed of 200 mm/s.

The process yields a metal to dielectric adhesion greater than 1 N/mm^2 and a silver layer conductivity of about $1.8 \times 10^6\sigma$ (S/m) measured at 20 °C. Electronic devices fabricated with this process have been tested to meet industrial-grade performance between −45 °C and 85 °C per IPC-2221B [7]. The current materials, printing resolution, and the process yield a top surface roughness of about $Sa = 1.7$ and $Sq = 2.1$ μm, Fig. 3, where Sa and Sq are the average and root mean roughness, respectively.

The dc dielectric constant was calculated from capacitance measured with a Keithley digital multi meter (DMM) 6500 and the distance between plates was measured by cross sectioning the test capacitor. The RF dielectric constant and losses were measured with Keysight P network analyzer (PNA) N5232B connected to a SPEAG dielectric assessment kit (DAK) 3.5-TL RF dielectric characterization unit (Fig. 4). The technique used by these dielectric characterization systems is based on microwave dielectric relaxation spectroscopy [8]. D_k varies from 2.91 to 2.69, while D_f varies from 0.024 to 0.015, as the frequency increases from 0.2 to 20 GHz, as summarized in Table I. The measured decrease in D_k and specially in D_f, as the frequency increases, is due to the dipole nature of the polymer. This behavior in the dielectric properties is influenced by the electronic, atomic, and orientational polarizations. These polarizations change with the changes in the electric

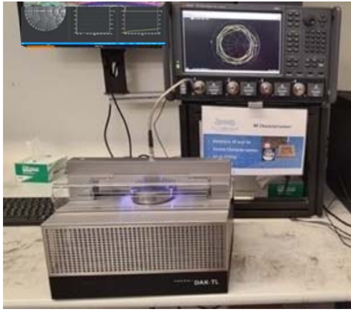
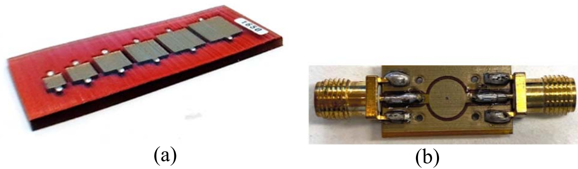


Fig. 4. Experimental setup for measuring RF dielectric parameters D_k and D_f.

TABLE I
MEASURED DC AND RF DIELECTRIC CONSTANT, D_k, AND LOSSES, D_f. THE ERROR OF THE MEASUREMENT IS LESS THAN 2% THREE SIGMA

Frequncy (GHz)	DC	0.2	0.5	1	2	5	10	15	20
Dielectric Constant (Dk)	3.33	2.91	2.87	2.84	2.75	2.82	2.78	2.77	2.69
Tangential loss x10^{-2} (Df)	-	2.4	2.1	2.5	1.5	2.5	1.7	1.9	1.5



(a) (b)

Fig. 5. (a) Photograph of an AME capacitor dc test coupon showing the contacts for each capacitor on opposite sides. (b) RF test coupon.

field [9]. Since the measurements are a bulk measurement in the Z-direction, they cannot be directly correlated with the roughness of the film in the x- or y-direction for the insertion losses that could be present in a transmission line.

B. Capacitor Tests and Results

The capacitors were characterized for the following: capacitance fabrication repeatability, dc voltage breakdown, ac and RF impedance stability, and Q-factor stability.

Fig. 5 shows both a dc test coupon as well as an ac/RF test coupon. Each dc test coupon consisted of six capacitors varying in area. For the purpose of testing the repeatability of the capacitors properties, each test coupon was printed with the same number of layers regardless of the area, while layer-specific capacitors were fabricated as well. The dc test results are summarized in Table II, while Fig. 6 shows the capacitance values as a function of area for each capacitor layer count and the number of layers as a parameter. Typical values are within 1 pF–3.4 nF. Lower capacity values are possible by increasing the thickness of the dielectric or reducing the area. The data are based on printing six capacitor coupons in at least six different printers and at least seven times per printer, which provided a capacitance repeatability greater than 98.5%.

TABLE II
DC TEST RESULTS SUMMARY

Capacitance Range	0.1 nF to 3.2 nF (at 25°C)
Capacitance Tolerances	<1.5%
Leakage current	<1 pA
Break down voltage (AC)	>1 kV
Temperature stability factor	25 °C-95 °C :0.2 [%/°C], 95° C-125 °C: 0.4 [%/°C]

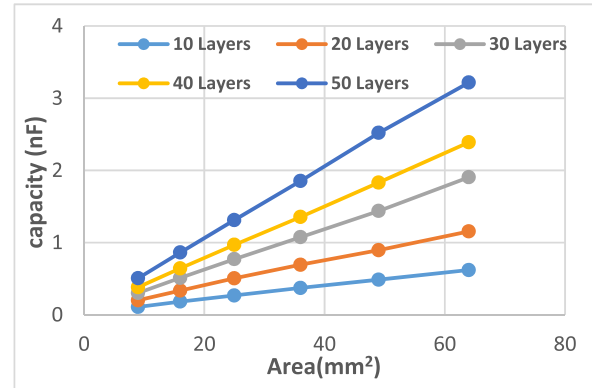


Fig. 6. Capacity value as a function of the area with the number of layers as a parameter. The measured values were repeatable to be within less than 1.5% for a minimum of 42 samples for each data point.

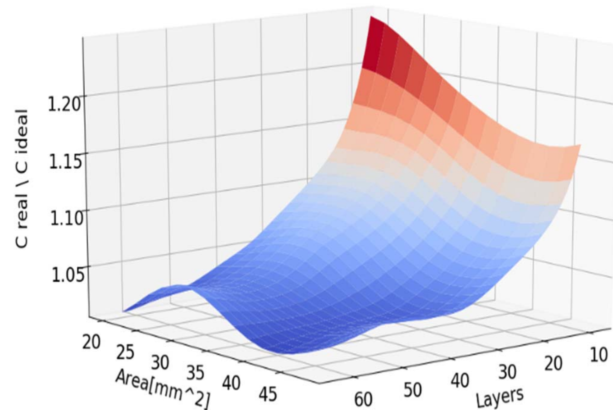


Fig. 7. Ratio between measured and calculated capacitance.

Fig. 7 shows the ratio between the actual measured capacitance (C_{real}) and the calculated one (C_{ideal}); the ratio is greater than 1. This can be attributed to two factors: edge effects of the capacitor's plates, and the difference between designed and actual dielectric which is less than 5% in layer thickness. As expected, the capacitors with the smaller area are more influenced by the edge effects, which becomes dominated by the reduced linearity of the electric field vector. The ratio between real to ideal capacitance is described as [10]

$$\frac{C_{\text{real}}}{C_{\text{Ideal}}} = 1 + 1.013 \times \frac{d}{l} \tag{2}$$

where d is the distance between two plates and l is the length of square plate. The test results show a 92% correlation between (2) and data, see Fig. 7.

Temperature stability between 25 °C and 125 °C in a dry environment was also characterized for these AME capacitors. With the samples in an oven, the capacitance was measured with a Keithley DMM. The results indicated that up to 95 °C, the capacitance increases at a rate of 0.2%/°C, while from 95 °C to 125 °C, this rate is 0.4%/°C. In either case, this rate of increase is an order of magnitude lower than the one in commercial capacitors, which is typically 1.2%/°C for high-quality devices [11]. The positive result is attributed to the temperature stability of the printed DI material.

The breakdown voltage was measured to be 1.1–1.35 kV (ac). This was measured on the capacitors by using an SCI 290 series high voltage measurement (HIPOT) tester. These results were observed on all the capacitors independent of area and number of layers. For reference, the dielectric material breakdown voltage measured by the National Institute of Standards and Test (NIST) according to IPC-TM-650 2.5.6 [12] yields a breakdown voltage of 40.3 kV on a 0.6-mm-thick dielectric sample. Since the volume resistivity of the material is linear within the dielectric, the breakdown voltage is also linear. This yields a thickness calculated breakdown voltage of 1.15-kV dc in agreement with the measured values. No leakage current was observed below the breakdown voltage, and no difference was observed between square- and round-shaped capacitor electrodes.

AC and RF testing from 1 kHz to 20 GHz, including Q-factor and impedance, were also performed. The performance of the AME capacitors was compared to commercial off-the-shelve ceramic capacitors [11]. The commercial capacitors were mounted on a similar coupon compensating for the contact pads. The printed capacitors were picked to have similar values to the commercial capacitors.

The measurements were divided into two tests.

1) DC up to 300 kHz with *LCR* Keysight E4980AL-032 for dissipation factor (DF) and impedance stability.
2) 300 kHz–20 GHz with a Keysight PNA 5232B. For calibration, open, short, and 50 Ω coupons with the same geometry as in Fig. 8 were used.
3) The capacitor Q-factor is defined as

$$Q = \frac{1}{DF}. \tag{3}$$

The DF was measured with a Keysight *LCR* meter E4980AL. Fig. 8 shows the average change in Q-Factor for AME and commercially available smaller capacitors in the 1–300-kHz frequency range. The minimized DF change in the AME capacity is an indication of better stability over the same range of frequencies, which is a relevant factor for RF applications [13].

Fig. 9(a) and (b) shows the impedance and phase change response for both AME and commercial capacitors in the 2–20 GHz range. Line A in Fig. 9(a) shows that for AME capacitors, the impedance increase is at higher frequencies compared to commercial capacitors. A closer look at the 50 MHz–3 GHz frequency range shows that the impedance for AME capacitors increases as the frequency increases at a factor 3× lower than for commercial capacitors, see Fig. 10. These effects are attributed to the lower parasitic components

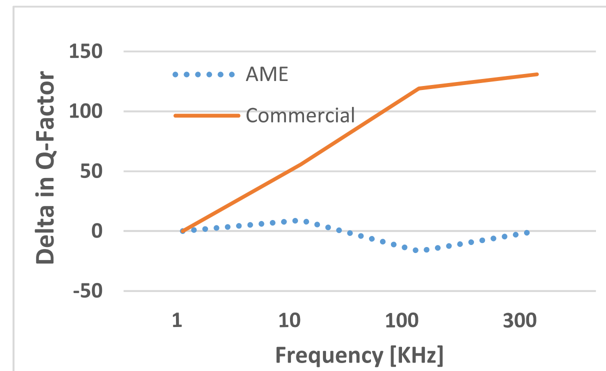


Fig. 8. Q-factor stability. Indication of the change in Q-factor as a function of frequency. AME capacitors essentially show no change as a function of frequency compared to commercial.

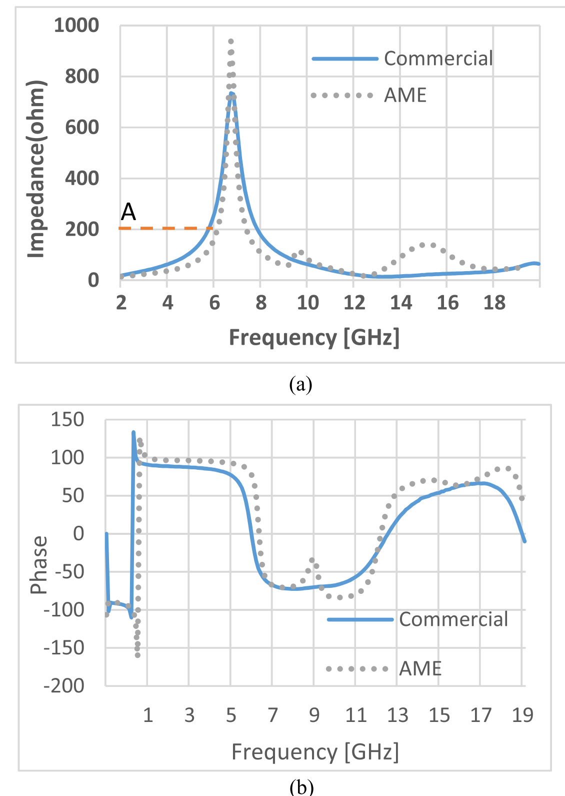


Fig. 9. RF response for both AME and commercial capacitors. (a) Impedance. Line A shows that the impedance of the AME capacitors increases at higher frequencies compared to the commercial ones. (b) Phase comparison.

in the AME capacitors due to the absence of soldering and packaging compared to commercial capacitors. For better understanding of the results, Fig. 11(a) and (b) shows the equivalent circuit for AME and commercial capacitors.

The difference between the two models is

1) AME capacitors exhibit the via connecting resistances, $R3$ and $R4$.
2) Commercial capacitors exhibit the parasitic effects of packaging: Cext1 and Lext1, external capacitance and inductance, respectively.

These models were confirmed by the simulation, using Applied Wave Research's (AWR) Design Environment [14].

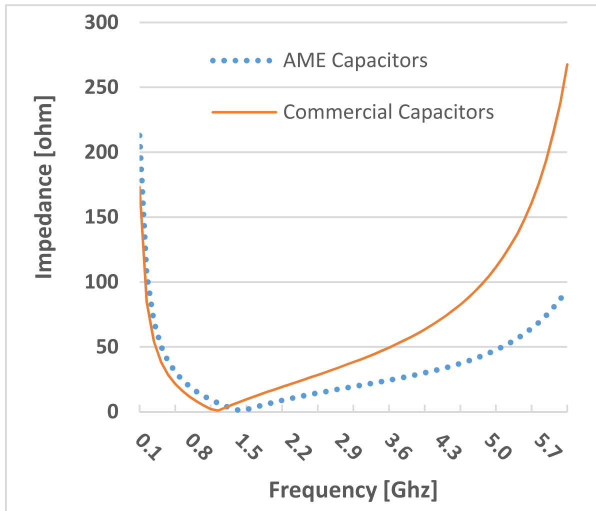


Fig. 10. RF response for 100 pF both AME and commercial capacitors from 50 MHz to 6 GHz. The AME capacitor impedance raises 3× slower than the commercial one with an increase in frequency.

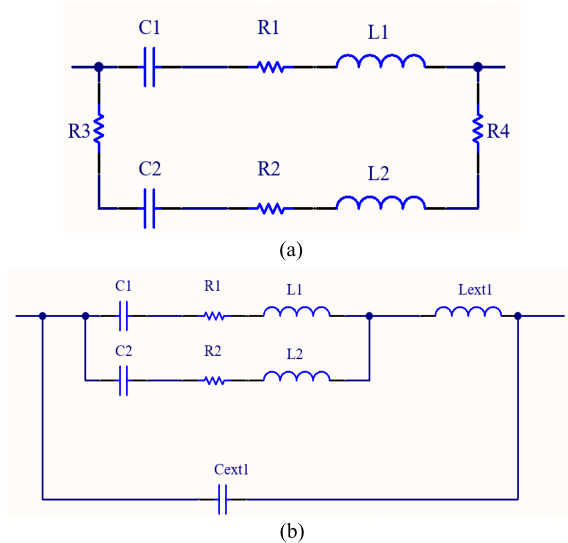


Fig. 11. Equivalent circuit diagram for (a) AME and (b) commercial capacitors including RF signal connection and terminal.

The measured impedance for both types of capacitors is with a nominal value of 7.5 pF (see Fig. 12). Simulation was used to calculate the values of the resistors, capacitors, and inductors, see Table III. The resulting low ESR values indicate that the roughness of the material does not affect the losses.

The data in Table III clearly show that the intrinsic commercial capacitor has resistances and inductances at least one and two orders of magnitude higher than the AME capacitor. Hence, at a frequency range of 100 kHz–6 GHz, AME capacitors exhibit an impedance that behaves more like theoretical impedance ($Z = (1/WC)$), therefore, simplifying the circuit design specially for RF applications. The lower resistance values also point to the use of the AME capacitors for high-power RF applications. The external values in Table III correlate to the printed test fixture and soldering the SubMiniature version A (SMA) connectors. There is an

TABLE III

CALCULATED VALUES FOR THE CAPACITORS' EQUIVALENT CIRCUITS

	Parameter	Unit	AME	Commercial
	Nominal value	pF	7.5	7.5
Intrinsic Capacitor	C1	pF	3.75	8.1
	R1	ohm	0.1	4
	L1	nH	0.05	0.32
	C2	pF	3.75	0.5
	R2	ohm	0.1	20
	L2	nH	0.05	0.4
	R3	ohm	0.1	0
	R4	ohm	0.1	0
Mounting and Test Parasitics	Cext	pF	0.68	0.68
	Lext	nH	2.2	2.5

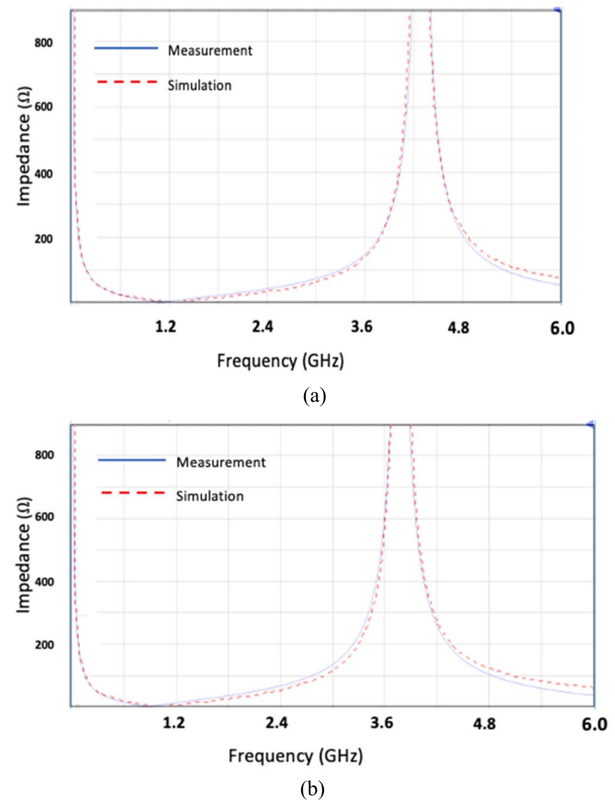


Fig. 12. Simulated and experimental impedance for a 7.5-pF (a) AME and (b) commercial capacitors.

external resistance not shown in the model since its value was calculated to be less than 0.1 Ω with no effect on the impedance and frequency behavior.

III. CONCLUSION AND DISCUSSION

AME circuits can benefit from the better performance demonstrated by capacitors manufactured as part of the electronic circuit board for both dc and RF frequencies. The AME capacitors show better performance for RF application than the equivalent commercial capacitors. Lower absolute impedance and lower impedance degradation over wide frequency ranges, lower ESR and ESL. This is driven by the properties of the AME dielectric, the elimination of soldering, and encapsulation required by commercial surface mount

device (SMD) devices. With regard to the printing process of the AME capacitor, it is important to ensure low resistance of the layer connection vias in order to maintain the RF benefits. As the capabilities of AME fabrication equipment are improved and more dielectric materials become available, the authors plan to study thinner dielectric thicknesses and combinations of dielectrics with different dielectric constants. This should enable smaller and larger capacitors, as well as achieving dielectric thicknesses of less than 10 μm. Furthermore, improving the silver nanoparticle conductivity will enable thinner layers and reduce the inductance effects. This will enable a full spectrum of capacitors not only for RF and high-speed logic but also for power applications enabled by the lower intrinsic resistance and inductances of the AME capacitors.

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